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isolate FET M3 313 from the resistively coupled base terminals of transistors Q1 301 and Q2 302. A voltage drop across resistor R3 333 matches the voltage drop across resistor R4 334.

Please replace paragraph [0026] with the following amended paragraph:

[0026] Miller feedback within the circuit is a result of the dominant pole formed by FET M3 313. A small change in current of FET M3 reflects back to its gate terminal through capacitor [[C1]] 341, where resistor R2 332 and capacitor [[C1]] 341 operate in conjunction as a voltage swing reduction circuit to reduce large voltage swings on the gate terminal of FET M3 313. Opposite to that which is provided by the prior art illustrated in FIG. 1, which provides no stabilization correction.

Please replace paragraph [0027] with the following amended paragraph:

[0027] In equilibrium, the drain current of FET M2 312 balances the current I_{in} sunked from the current sink 321 and the potential on the drain of FET M2 312 biases the gate terminal of FET M3 313. This causes current flow in the drain terminal of FET M3 313, which drives the base terminals of transistors Q1 301 and Q2 302. The resultant collector terminal current in transistor Q1 301 drives the second [[first]] current mirror port 305b, through the first current ratio port 306a, and causes current to flow in the drain terminal of FET M2 312. By making FET M1 311 N times wider than FET M2 312 the current in the collector terminal of transistor Q1 301 is N times larger than the current in the drain terminal of FET M2 312. By making transistor Q2 302 M times larger than transistor Q1 301 the current in the collector terminal of transistor Q2 302 is M times larger than the current in the collector terminal of transistor Q1 301. Thus, the mean current propagating through the load resistor, [[R1]] 331 from the second ratio output port 306b, is $M*N*I_{in}$ when there is no RF modulation provided to the circuit via the RF input port 300c.

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Please replace paragraph [0027] with the following amended paragraph:

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9-18-06